

ABSTRACT OF THE DISCLOSURE

Logic circuits that support the addition of three binary numbers using hardwired adders are described. In one embodiment, this is accomplished by using a 3:2 compressor (i.e., a Carry Save Adder method), using hardwired adders to add the sums and carries produced by the 3:2 compression, and sharing carries data calculated in one logic element ("LE") with the following LE. In such an embodiment, with the exception of the first and last LEs in a logic array block ("LAB"), each LE in effect lends one look-up table ("LUT") to the LE below (i.e., the following LE) and borrows one LUT from the LE above (i.e., the previous LE). The LUT being lent or borrowed is one that implements the carry function in the 3:2 compressor model. In another aspect, an embodiment of the present invention provides LEs that include selectors to select signals corresponding to the addition of three binary numbers mode.